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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/476,622 | 12/31/1999 | Howard Chin | 884.101US1 | 8079 |

8791 7590 01/20/2006

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| EXAMINER | |
|---|---|
| TREAT, WILLIAM M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/476,622 | CHIN ET AL. | |
| | Examiner | Art Unit | |
| | William M. Treat | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *21 and 29-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21 and 29-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 21 and 29-40 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. As to claim 31, applicants make clear on page 8 of their original specification that their system has an instruction that can move a value from a machine specific register to a general purpose register and an instruction that can move a value from a general purpose register to a machine specific register. Claim 31 is worded as if applicants have an instruction to move a value from one machine specific register to another machine specific register which is not found in applicants' original disclosure. Claim 31 represents new matter and should be cancelled.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As to claim 31, see paragraph 4, *supra*, for an explanation.

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

9. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 21 and 29-40 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-32 of copending Application No. 10/304,199. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

11. The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: Claims 13 and 21-32 of Application No. 10/304,199 are virtual duplicates of claims 21 and 29-40, respectively.

12. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other

copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 21 and 29-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Margulis (i860 Microprocessor Architecture) in view of Carbine et al. (Patent No. 5,222,244).

16. Margulis substantially taught the invention of exemplary claim 21 including a system, comprising: a bus (Figs.3-1, p. 35 and 8-10, p. 232); a processor (Figs.3-1 and 8-10, p. 232) including a plurality of machine specific registers (Fig. 8-10 and pp. 80-99, psr, epsr, db, dirbase, fir, and, fsr), wherein each one of the plurality of machine specific registers is associated with one or more functional units (pp. 34-36) of the processor;

said processor to execute an instruction that updates at least one instruction by changing a value of at least one bit in at least one of said plurality of machine specific registers (pp. 251-253); and a computer readable medium external to the processor (external memory, Fig. 8-10, p. 232) and coupled to the processor by the bus (Fig. 8-10, p. 232), the computer readable medium to store said instruction.

17. Margulis taught his instructions were RISC instructions (p. 3). He did not teach his instructions were microinstructions. However, Carbine taught using RISC instructions as microinstructions was old and well-known in the art (col. 8, lines 15-25). One of ordinary skill is motivated to use RISC instructions as microinstructions because of their compatibility with current trends in design, fabrication and compiler technologies. One would be motivated to apply Margulis' teachings (such as modifying the RM bits in the floating point status register (pp. 90-92) and having the fix and pfix instructions (p. 140) round based on the value in RM) to a system with RISC microinstructions because it affords flexibility in the instruction set, as when four different modes of rounding are handled by one instruction, without modifying that instruction and without having a different instruction for each rounding mode. Also, there is a huge existing market for personal computer (PC) systems which convert X86 instructions into RISC-type microinstructions for running on newer non-X86 hardware.

18. Applicants have chosen an entirely generic computer system as the environment for their claim 13 and their other claims. In describing on pages 3-4 their computer system represented by Fig. 1, applicants recite only conventional devices and even recite multiple alternative conventional devices for their categories of device. Since

applicants' computer environment is merely conventional equipment configured as one of ordinary skill would be motivated to do so, the examiner has accorded it little weight in terms of providing patentable differentiation.

19. As to claim 29, it differs from rejected claim 21 only in its mention of controlling one of the at least two functional units in response to executing said updating instruction. The floating point functional unit of Margulis would be appropriately controlled as discussed in paragraph 17, *supra*.

20. As to claim 30, Margulis taught a method wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor. Logically, if a functional unit can read and/or write some portion of a register's contents then that register must be associated with that functional unit. Margulis taught modifying the RM bits in the floating point status register (pp. 90-92) and having the floating point fix and pfix instructions (p. 140) round based on the value in RM. He also taught RISC core instructions ld.c and st.c are used to modify the RM bits (pp. 251-253).

21. As to claim 31, Margulis taught a method wherein a logical source register for executing an instruction (ld.c) and a logical destination register for executing a different instruction (st.c) are selected from the plurality of machine specific registers (pp. 251-253) which is all applicants actually taught in their original disclosure (p. 8 of applicants' specification).

22. As to claim 32, it fails to teach or distinguish over rejected claims 21 and 29-31.

23. As to claims 33-34, Margulis taught controlling a non-performance critical function selected from the group consisting of: cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions. Margulis taught modifying the RM bits in the floating point status register (pp. 90-92) and having the floating point fix and pfix instructions (p. 140) round based on the value in RM.

24. As to claim 35, it fails to teach or distinguish over rejected claims 13-26.

25. As to claim 36, Margulis taught the article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing: moving a value from a general purpose register of the processor to the one or more machine specific registers (st.c, pp. 251-253)

26. As to claim 37, the examiner takes Official Notice that firmware storing external microcode that was subsequently fetchable was known to one of ordinary skill in the art at the time of applicants' invention as were the benefits (such as greater ability to adapt to later design changes) of using external, modifiable microcode in firmware.

27. As to claims 38-40, they fail to teach or define over rejected claims 21 and 29-37 in any substantive way.

28. As best the examiner can tell because of applicants' rather limited disclosure, applicants and their assignee seem to have borrowed a concept from the Intel i860 microprocessor and claimed it as a new invention without bothering to mention

assignee's related art to the examiner. Modifying the RM bits in the floating point status register (pp. 90-92) and having the fix and pfix instructions (p. 140) round based on the value in RM sure sounds like the concept being claimed by applicants though applicants' imprecise verbiage obscures the nature of their claimed invention. The only difference seems to be that the i860 uses a RISC instruction set directly as opposed to some combination of complex instructions and what are probably RISC microinstructions being used in applicants' system. Anyone of ordinary skill in the art at a company like Intel, IBM, AMD, etc. could readily adapt the concept. One of ordinary skill would be motivated to adapt the concept because it affords flexibility in the instruction set, as when four different modes of rounding are handled by one instruction without modifying that instruction and without having a different instruction for each rounding mode.

29. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER